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EXAMINER	
PIZIALI, JEFFREY J	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/026,406	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Jeff Piziali	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 July 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-4,7-18,20,25,26,31-62,65-67 and 72* is/are pending in the application.

4a) Of the above claim(s) *2-4,8-14,20,25,26,31-36,38-62 and 65-67* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7,15-18,37 and 72* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 December 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 26 July 2010 has been entered.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Terminal Disclaimer

3. The terminal disclaimer filed on 30 April 2007 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of **US Patent Number 6,975,298** has been reviewed and is accepted. The terminal disclaimer has been recorded.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 7, 15-18, 37, and 72 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "**n is a natural number**" (line 4). It is respectfully noted that zero is a natural number.

For example: it would be unclear to one having ordinary skill in the art whether the claimed "n first memories," "n second memories," "n bit digital video signals," and "n counter signals" are actually necessary elements of the claimed invention (if n = 0).

An omitted structural cooperative relationship results from the claimed subject matter: "**different frequencies**" (line 18).

It would be unclear to one having ordinary skill in the art what the frequencies are intended to be different from.

7. Claim 7 recites the limitation "**at the same time as the first reset signal**" (line 22). There is insufficient antecedent basis for this limitation in the claim.

It would be unclear to one having ordinary skill in the art what this limitation is intended to mean. "At the same time as the first reset signal" does what?

8. Claim 15 recites the limitation "**the other**" (line 6). There is insufficient antecedent basis for this limitation in the claim.

9. Claim 15 recites the limitation "**each of the output terminals**" (line 8). There is insufficient antecedent basis for this limitation in the claim.

10. Claim 15 recites the limitation "**third information**" (line 10). There is insufficient antecedent basis for this limitation in the claim.

11. Claim 15 provides for the use of the NOR (line 11), but, since the claim does not set forth any steps involved in the method/process, it is unclear what method/process applicant is intending to encompass. A claim is indefinite where it merely recites a use without any active, positive steps delimiting how this use is actually practiced.

Claim 15 is rejected under 35 U.S.C. 101 because the claimed recitation of a use, without setting forth any steps involved in the process, results in an improper definition of a process, i.e., results in a claim which is not a proper process claim under 35 U.S.C. 101. See for example Ex parte Dunki, 153 USPQ 678 (Bd.App. 1967) and Clinical Products, Ltd. v. Brenner, 255 F. Supp. 131, 149 USPQ 475 (D.D.C. 1966).

12. Claim 15 recites the limitation "**the first information**" (line 11). There is insufficient antecedent basis for this limitation in the claim.

13. Claim 15 recites the limitation "**the second information**" (line 12). There is insufficient antecedent basis for this limitation in the claim.

14. Claim 16 recites the limitation "**the other**" (line 5). There is insufficient antecedent basis for this limitation in the claim.

15. Claim 16 recites the limitation "**third information**" (line 6). There is insufficient antecedent basis for this limitation in the claim.

16. Claim 16 recites the limitation "**the first information**" (line 6). There is insufficient antecedent basis for this limitation in the claim.

17. Claim 16 recites the limitation "**the second information**" (line 8). There is insufficient antecedent basis for this limitation in the claim.

18. Claim 18 recites the limitation "**the highest**" (line 4). There is insufficient antecedent basis for this limitation in the claim.

19. Claim 15 recites the limitation "**the lowest**" (line 5). There is insufficient antecedent basis for this limitation in the claim.

20. The remaining claims are rejected under 35 U.S.C. 112, second paragraph, as being dependent upon rejected base claims.

21. The claims are rejected under 35 U.S.C. 112, second paragraph, as being indefinite.

As a courtesy to the Applicant, the examiner has attempted to also make rejections over prior art -- based on the examiner's best guess interpretations of the invention that the Applicant is intending to claim.

However, the indefinite nature of the claimed subject matter naturally hinders the Office's ability to search and examine the application.

Any instantly distinguishing features and subject matter that the Applicant considers to be absent from the cited prior art is more than likely a result of the indefinite nature of the claims.

The Applicant is respectfully requested to correct the indefinite nature of the claims, which should going forward result in a more precise search and examination.

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any

evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

24. Claims 7, 17, and 72 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kurumisawa et al (JP 11-295700 A)** in view of **Sato et al (US 5,712,652 A)** and **Okumura et al (US 5,945,972 A)**.

Please note: An English translation of the **Kurumisawa** reference was included with the 24 March 2010 Office action, and the translation has been relied upon in the following rejections.

Regarding claim 7, **Kurumisawa** discloses a method of driving a light emitting device [e.g., Fig. 1], said light emitting device including

a plurality of pixels [e.g., Fig. 1: P11, P21], each of the plurality of pixels comprising:

~~n first memories~~ (n is a natural number);

n second memories [e.g., Figs. 1, 2: 6];

a display signal generating portion [e.g., Figs. 1, 3: 7];

a counter circuit [e.g., Fig. 3: P0-P7; Fig. 7: 601];

a light emitting element [e.g., Fig. 1: 3]; and

a current controlling thin film transistor [e.g., Fig. 3: 7b];

said method comprising the steps of:

~~sequentially writing each bit of n bit digital video signals in each of the n first memories;~~

writing each bit of the n bit digital video signals [e.g., Fig. 1: video signals on data lines D] ~~which have been written in each of the n first memories~~, in each of the n second memories at once;

inputting [e.g., Fig. 3: RAM1-RAM8] each bit of the n bit digital video signals, which have been written in each of the n second memories, to the display signal generating portion;

starting an output of n counter signals [e.g., Fig. 7: Q1-Q8] from the counter circuit in response to a first reset signal [e.g., Fig. 7: 603 output],

the n counter signals having different frequencies [e.g., see Fig. 8: Q0, Q1] respectively;

inputting [e.g., Fig. 3: P0-P7] the n counter signals to the display signal generating portion; and

inputting a display signal [e.g., Fig. 3: XQ via 14] into a gate electrode [e.g., Fig. 3: gate of 7b] of the current controlling thin film transistor in response to a second reset signal [e.g., Fig. 3: YD] at the same time as the first reset signal (see the entire document, including Paragraphs 34-87).

Kurumisawa does not appear to expressly disclose sequentially writing each bit of n bit digital video signals in each of the n first memories, as instantly claimed.

However, **Sato** does disclose sequentially writing each bit of n bit digital video signals [e.g., Fig. 2: video signals on line 203] in each of n first memories [e.g., Fig. 2: 204]; and then

writing each bit of the n bit digital video signals which have been written in each of the n first memories, in each of n second memories [e.g., Fig. 1: 100] at once (see the entire document, including Column 12, Line 50 - Column 13, Line 42).

Kurumisawa and **Sato** are analogous art, because they are from the shared inventive field of driving liquid crystal displays.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use **Sato's** first memories [e.g., Fig. 2: 204] to feed **Kurumisawa's** [e.g., Figs. 1, 2: 6], so as to write data to the data line pairs only when video image data has changed, thereby reducing power consumption.

Sato does not appear to expressly disclose each of the plurality of pixels comprising the first memories, as instantly claimed.

However, **Okumura** does disclose each of a plurality of pixels comprising:

a plurality of memories [e.g., Fig. 3: 121a, 121b] and controlling circuitry [e.g., Fig. 3: 123, 124] for writing data only when video image data has changed -- again for reducing power consumption, just like **Sato** (see the entire document, including Column 12, Line 41 - Column 17, Line 20).

Additionally, **Okumura** discloses that it was known in the art to substitute an electroluminescent element in the place of a liquid crystal element (e.g., see Column 28, Lines 4-11).

Kurumisawa, **Sato**, and **Okumura** are analogous art, because they are from the shared inventive field of driving liquid crystal displays.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use **Okumura's** technique of placing image-change-detecting memory circuitry within pixels so as to move **Sato's** first memories [e.g., Fig. 2: 204] to be located within **Kurumisawa's** pixels [e.g., Fig. 1: P11, P21], so as reduce the number of column lines traversing the display panel.

Moreover, it would have been obvious to one of ordinary skill in the art at the time of invention because all the claimed elements were known in the prior art and one skilled in the art could have located additional memories within the pixels as claimed by known methods with no change in their respective functions, and the combination would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

Should it be shown that **Kurumisawa's** switching circuit [e.g., Fig. 3: 7b] teaches a current controlling thin film transistor, as claimed, with insufficient specificity:

Kurumisawa discloses using a current controlling thin film transistor [e.g., Fig. 13: illustrated TFTs] as a switching circuit (e.g., see Page 3, Paragraph 2).

Sato also discloses using a current controlling thin film transistor [e.g., Fig. 1B: 6, 7] as a switching circuit (e.g., see Column 9, Line 40).

Okumura additionally discloses using a current controlling thin film transistor [e.g., Fig. 1B: SW] as a switching circuit (e.g., Column 9, Line 55).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use a current controlling thin film transistor (as taught by **Okumura**, **Sato**, and/or **Kurumisawa**) to form **Kurumisawa's** switching circuit [e.g., Fig. 3: 7b], so as to make use of an inexpensive, well known, commonly understood, readily available, and frequently used type of switch.

Regarding claim 17, **Kurumisawa** discloses each of the ~~first memories and~~ second memories is an SRAM [e.g., Fig. 2: 6] (see the entire document, including Paragraph 42).

Moreover, it would have been obvious to one having ordinary skill in the art at the time of invention to use **Kurumisawa's** SRAM [e.g., Fig. 2: 6] to form **Sato's** first memories [e.g., Fig. 2: 204], because all the claimed elements were known in the prior art and one skilled in the art could have used SRAM as claimed by known methods with no change in their respective functions, and the combination would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

Regarding claim 72, **Kurumisawa** discloses the light emitting element emits a light only during a period [e.g., Fig. 4: ONW] that starts with the start of the output of the n counter signals and

ends [e.g., Fig. 4: OFFW] as a plurality of first information of each bit of the n bit digital video signals inputted to the display signal generating portion matches a plurality of second information of each of the n counter signals

(see the entire document, including Paragraphs 34-87)

25. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Kurumisawa et al (JP 11-295700 A)**, **Sato et al (US 5,712,652 A)**, and **Okumura et al (US 5,945,972 A)** as applied to claim 7 above, and further in view of **Honig (US 3,903,857 A)**.

Regarding claim 15, **Kurumisawa** discloses the display signal generating portion has a ~~NOR~~ multiple input AND-gate [e.g., Fig. 7: 12] and n exclusive ORs [e.g., Fig. 7: 11],

wherein each of the n exclusive ORs has two input terminals,

wherein one of the input terminals [e.g., Fig. 3: RAM1-RAM8] is inputted with each bit of the n bit digital video signals inputted to the display signal generating portion

while the other [e.g., Fig. 3: P0-P7] is inputted with the n counter signals,

wherein each of the output terminals of the n exclusive ORs is all connected to an input terminal of the ~~NOR~~ multiple input AND-gate,

wherein third information of signals outputted from an output terminal of the ~~NOR~~ multiple input AND-gate is used to judge whether or not the first information of each bit of the n bit digital video signals inputted to the display signal generating portion matches the second information of each the n counter signals inputted to the display signal generating portion (see the entire document, including Paragraphs 34-87).

Kurumisawa does not appear to expressly disclose a NOR, as instantly claimed.

However, **Honig** does disclose substituting a NOR-gate in the place of a multiple input AND-gate (see the entire document, including Column 13, Lines 1-10).

Kurumisawa and **Honig** are analogous art, because they are from the shared inventive field of logic gate circuitry implementation.

It would have been obvious to one of ordinary skill in the art at the time of invention, because the substitution of one known NOR gate for another multiple input AND-gate would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

26. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Kurumisawa et al (JP 11-295700 A)**, **Sato et al (US 5,712,652 A)**, and **Okumura et al (US 5,945,972 A)** as applied to claim 7 above, and further in view of **Kondo (US 4,373,415 A)**.

Regarding claim 16, **Kurumisawa** discloses the display signal generating portion has an ~~R-S~~ D flip-flop circuit [e.g., Fig. 7: 14],

wherein the ~~R-S~~ D flip-flop circuit has two input terminals,

wherein one of the input terminals is inputted with reset signals [e.g., Fig. 7: YD]

while the other is inputted with signals having third information whether or not the first information [e.g., Fig. 7: via 13] of each bit of the n bit digital video signals inputted to the display signal generating portion matches the second information of each of the n counter signals inputted to the display signal generating portion,

wherein signals outputted from an output terminal of the ~~R-S~~ D flip-flop circuit causes the light emitting element to emit a light only during a period that starts with the start of output of the n counter signals and

ends as the first information of each bit of the n bit digital video signals inputted to the display signal generating portion matches the second information of each of the n counter signals (see the entire document, including Paragraphs 34-87).

Kurumisawa does not appear to expressly disclose a R-S flip-flop, as instantly claimed.

However, **Kondo** does disclose substituting an R-S flip-flop in the place of a D flip-flop (see the entire document, including Column 3, Lines 8-9).

Kurumisawa and **Kondo** are analogous art, because they are from the shared inventive field of flip-flop circuitry implementation.

It would have been obvious to one of ordinary skill in the art at the time of invention, because the substitution of one known R-S flip-flop for another D flip-flop would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

27. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Kurumisawa et al (JP 11-295700 A)**, **Sato et al (US 5,712,652 A)**, and **Okumura et al (US 5,945,972 A)** as applied to claim 7 above, and further in view of **Kobayashi (US 4,262,352 A)** and **Kinghorn (US 4,574,386 A)**.

Regarding claim 18, **Kurumisawa** discloses clock signals [e.g., Fig. 7: f1] are inputted to the counter circuit, and

wherein frequencies of the n counter signals arranged in order from the highest to the lowest correspond to 1/2, $1/2^2$,..., $1/2^n$ of frequencies [e.g., Fig. 8: Q0, Q1] of the clock signals, respectively (see the entire document, including Paragraphs 34-87).

Kurumisawa does not appear to expressly disclose plural clocks, as instantly claimed.

However, **Kobayashi** does disclose clock signals [e.g., Fig. 4: I_{69}, I_{12}] are inputted to a counter circuit [e.g., Fig. 4: 3] (see the entire document, including Column 12, Lines 45-50).

Additionally, **Kinghorn** discloses clock signals [e.g., Fig. 4: CP, inverse CP] are inputted to a counter circuit [e.g., Fig. 4] (see the entire document, including Fig. 10; Column 6, Line 5 - Column 7, Line 40).

Kurumisawa, **Kobayashi** and **Kinghorn** are analogous art, because they are from the shared inventive field of counter circuitry implementation.

It would have been obvious to one of ordinary skill in the art at the time of invention because all the claimed elements were known in the prior art and one skilled in the art could have input a counter with a pair of opposing phase clock signals as claimed by known methods with no change in their respective functions, and the combination would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

28. Claim 37 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Kurumisawa et al (JP 11-295700 A)**, **Sato et al (US 5,712,652 A)**, and **Okumura et al (US 5,945,972 A)** as applied to claim 7 above, and further in view of **Ouderkirk et al (US 6,124,971 A)**.

Regarding claim 37, **Sato** does not appear to expressly disclose an electroluminescence display device, as instantly claimed.

However, **Okumura** discloses that it was known in the art to substitute an electroluminescent element in the place of a liquid crystal element (e.g., see Column 28, Lines 4-11).

Additionally, **Ouderkirk** discloses an electroluminescence display device serving as a light source for a reflective liquid crystal display (see the entire document, including Column 1, Lines 40-60).

Kurumisawa, **Okumura** and **Ouderkirk** are analogous art, because they are from the shared inventive field of liquid crystal display devices.

It would have been obvious to one of ordinary skill in the art at the time of invention, because the substitution of one known electroluminescence display device for another liquid crystal display device would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

Moreover, it would have been obvious to one of ordinary skill in the art at the time of invention to use **Ouderkirk's** electroluminescence display device as a light source for **Sato's**

reflective LCD, so to as to provide supplemental electroluminescent light for low ambient light conditions.

Response to Arguments

29. Applicant's arguments filed on 26 July 2010 have been fully considered but they are not persuasive.

The Applicant contends, "In order to advance the prosecution of this application, Applicants are amending independent Claim 7 to recite the feature of 'inputting a display signal into a gate electrode of the current controlling thin film transistor in response to a second reset signal at the same time as the first reset signal.' This feature is supported by, for example, paragraph [0193] in the publication of the present application (US 2002/0130828)... While Applicants traverse these rejections, as explained above, in order to advance the prosecution of this application, Applicants are amending independent Claim 7. None of the cited references disclose or suggest this feature of Claim 7" (see Pages 29-30 of the Response filed on 26 July 2010). However, the examiner respectfully disagrees.

Kurumisawa discloses inputting a display signal [e.g., Fig. 3: XQ via 14] into a gate electrode [e.g., Fig. 3: gate of 7b] of the current controlling thin film transistor [e.g., Fig. 3: 7b] in response to a second reset signal [e.g., Fig. 3: YD] at the same time as the first reset signal [e.g., Fig. 7: 603 output] (see the entire document, including Paragraphs 34-87).

Applicant's arguments with respect to claims 7, 15-18, 37, and 72 have been considered but are moot in view of the new ground(s) of rejection.

By such reasoning, rejection of the claims is deemed necessary, proper, and thereby maintained at this time.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (571)272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on (571) 272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jeff Piziali/
Primary Examiner, Art Unit 2629
14 January 2011